The linearization of high-efficiency three-way Doherty Amplifier

Aleksandar Atanasković, Nataša Maleš-Ilić and Bratislav Milovanović

***Abstract* — Three-way Doherty amplifier in configuration with two quarter-wave impedance transformers in output combining circuit and with LDMOSFETs in carrier and peaking amplifies in periphery relations 1:2.5:2.5 has been linearized in this paper. The linearization has been performed by the fundamental signals' second harmonics (IM2) and fourth-order nonlinear signals (IM4). The peaking cells that operate at different bias conditions generate the signals for linearization (IM2+IM4). Those signals produced at the output of one peaking cell are directed to the input of the carrier amplifier, whereas ones generated at the output of another peaking cell are led to the carrier amplifier output. The linearization technique applied results in the suppression of the third- and fifth order intermodulation products of Doherty amplifier which delivers high efficiency.**

Keywords – **Doherty amplifier, linearization, power added efficiency, second harmonics, fourth-order nonlinear signals**

I. INTRODUCTION

More than ever, the modern wireless communication industry has increased interest for the high-efficient and linear amplifiers to accommodate current communication standards. The third generation (3G) and beyond communication standards offer high data rate transmission and transmit power that carries high-peak-to-average ratio signals. Therefore, base-station amplifiers operate most of their time at lower power level than their maximum, which consequently degrades the efficiency. The Doherty amplifier that is capable of achieving the requirements of the power amplifiers in base station concerning high efficiency becomes attractive for wireless industry.

The linearity of high power Doherty amplifier was improved using "post-distortion-compensation" [1], the feedforward linearization technique [2], the predistortion linearization technique [3] and combination of those two linearization techniques [4].

The linearization technique that utilizes the fundamental signals' second harmonics (IM2) and fourth-order nonlinear signals (IM4) at frequencies that are close to the second harmonics in order to suppress the third- and fifth-order intermodulation products (IM3 and IM5) of microwave amplifiers was investigated and applied in [5]-[6].

In the paper [7], for the first time, two-way conventional Doherty amplifier was linearized by applying an approach where IM2 and IM4 signals are injected together with the fundamental signals into the carrier amplifier input and put at its output. The signals for linearization are generated at the output of the peaking amplifier in Doherty configuration. The result is very good reduction of IM3 products accompanied with the high efficiency of Doherty amplifier, whereas the IM5 products cannot be suppressed at all.

The linearization of three-way Doherty amplifier in configuration with one quarter-wave impedance transformer in the output combining circuit and with LDMOSFETs in carrier and peaking amplifies in periphery relations 1:1:1 was considered in paper [8]. The linearization approach mentioned above achieved very good results in the reduction of both IM3 and IM5 products retaining the high efficiency of Doherty amplifier

In this paper three-way Doherty amplifier in the configuration with two quarter-wave impedance transformers in the output combining circuit [9]-[10] with transistor size ratio 1:2.5:2.5 is linearized. The output impedances of the amplifier cells are selected to satisfy the output power relations between the carrier and peaking cells. Also, the transmission lines in the output combining circuit should be practical for realization with not too high or too low characteristic impedances. The signals for linearization (IM2 and IM4) are extracted at the output of the peaking cells in Doherty amplifier that are biased at various points to provide the appropriate power levels and phase relations of IM2 and IM4 signals. After been adjusted in amplitude and phase the signals from the output of one peaking amplifier are injected at the input of carrier amplifier while ones appeared at the output of another peaking cell are put to the carrier amplifier output.

Section II includes the design of three-way Doherty amplifier and all results referring to the intermodulation products and efficiency obtained in simulation for two sinusoidal as well as digitally modulated signals by applying the linearization approach.

II. THREE-WAY DOHERTY AMPLIFIER

In a classical Doherty amplifier operation high efficiency is obtained over a range of 6dB below maximum output power. The concept of multistage Doherty amplifier is used to maintain the efficiency in the backoff region that can be extended beyond the classical design.

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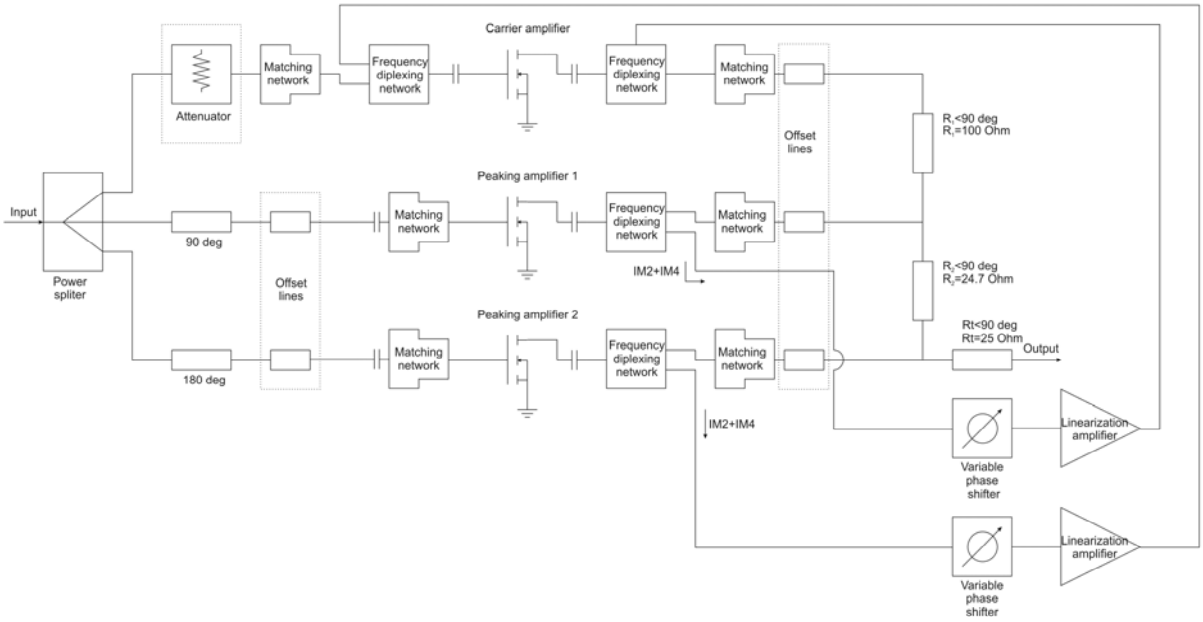

Fig. 1. Three-way Doherty amplifier with additional circuit for linearization

A. Design

The output impedances of the amplifier cells should be chosen to satisfy the output power relations between the carrier and peaking cells, [9]. However, it should draw attention to the fact that too high or too low characteristic impedances of transmission lines in the output combining circuit are unpractical for realization. Therefore, for the output impedance of carrier amplifier 100Ω was selected, whilst 40Ω and 30Ω are set for the output impedances of two peaking amplifiers. Consequently, according to the analysis performed in [10], the characteristic impedances of the quarter-wave transformers in output combining network were found to be $R_1 = 100\Omega$, $R_2 = 24.74\Omega$, while the quarter-wave transformer with characteristic impedance $R_t = 25\Omega$ transforms 50Ω to 15Ω as shown in Fig. 1.

The peaking amplifiers that are forced to operate in class-C have tipically lower gain compared to the class-AB of carrier amplifier. Therefore, the periphery of the peaking amplifiers needs to be enlarged to compensate for the gain reduction in the class-C amplifiers. The device periphery calculated for the determined back-off levels (6dB and 12dB) resultes in a ratio 1:3:4, [9]-[10]. However, the choice was limited by the device availability so that 1:2.5:2.5 device size ratio was selected.

The carrier amplifying cell was designed using Freescale's MRF281SR1 LDMOSFET with a 4-W peak envelope power level (PEP) according to the non-linear MET model included in ADS library. The matching impedances for source and load at 2.14GHz are $Z_s = 3.1 - j3.5\,\Omega$ and $Z_L = 11.36 + j7.94\,\Omega$, respectively. A quiescent bias for class-AB is set to $V_G = 5.1\text{V}$ (13.5%I_{DSS}) and the drain bias voltage $V_D = 26\text{V}$ is the same for all amplifiers.

For the peaking cells Freescale's MRF282S LDMOSFET was utilized. Non-linear MET model included in ADS library exhibits a 10-W peak envelope power level. The peaking amplifiers 1 and 2 were set to operate at class-C, V_G=3.2V and V_G=1.5V, respectively. The matching impedances of MRF282S LDMOSFET for source and load at 2.14GHz are $Z_S = 1.85 + j1.6\,\Omega$ and $Z_L = 3.55 - j0.2\,\Omega$.

The input matching was performed for 50Ω, while the output matching circuits were designed to transform the optimum output impdance of the carrier and two peaking cells to 100Ω, 40Ω and 30Ω, respectively.

Offset lines are incorporated at the output of peaking amplifier cells to minimize the effective loading of the peaking amplifiers in state when those amplifiers do not operate (low-power range). The insertion of 40Ω line at the output of the peaking amplifier 1 and 30Ω line at the output of the peaking amplifier 2 will not only rotate output impedances of the peaking cells to as high as possible values but will also change the phase of the peaking amplifiers when they are active, distorting the desired phase relations in Doherty amplifier. If the delay lines are inserted at the input of the peaking amplifiers or an appropriated offset line is adjusted at the output of the carrier amplifier the compensation of the phase discrepancies can be carried out.

The length of offset lines at the peaking amplifer output circuits determined to lower leackage current at low-power region are 5° and 15°. In order to compensate for the phase variaty at the output combining circuit the signals at the input of the peaking amplifiers were delayed for the appropriate values.

According to the analysis performed in [11] Doherty amplifier with uneven power drive of the carrier and peaking cells operates more linear and generates full power from both amplifiers producing in that way more power than configuration with identical power level. Therefore, the peaking amplifiers were driven by signals with 1dB higher power than that of the carrier amplifier. Maximum output power achieved by this Doherty configuration is 44dBm.

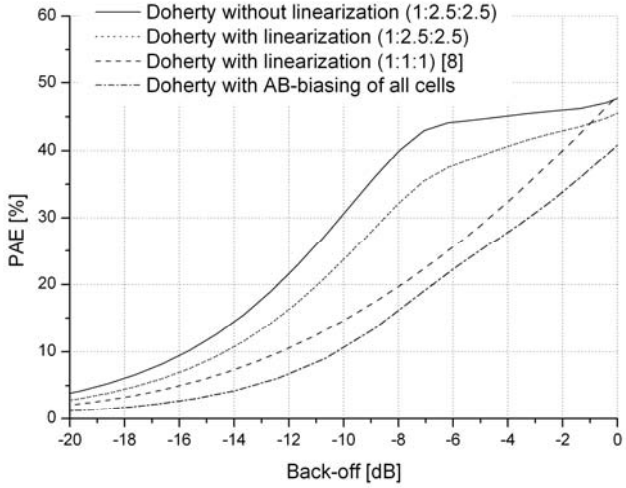

Fig. 2. Power added efficiency of three-way Doherty amplifier for device size ratio 1:2.5:2.5

Power added efficiency for the designed three-way Doherty amplifier is presented in Fig. 2 showing considerably better PAE characteristic (21.9% higher at 6dB back-off) in comparison with the class-AB amplifier obtained with AB-biasing of all cells in Doherty configuration.

B. Linearization

Theoretical analysis of the linearization approach that uses IM2 and IM4 signals for linearization has been given in [8]. It is based on the nonlinearity of drain-source current expressed by a polynomial model up to the fifth-order.

According to this, it is possible to reduce spectral regrowth caused by the third-order distortion of fundamental signal by choosing the appropriate amplitude and phase of IM2 signals injected at the input and output of the amplifier.

Additionally, the fifth-order intermodulation products can be reduced by adjusting the amplitude and phase of IM4 signals that are injected at the input of amplifier and put at its output.

The IM2 and IM4 signals generated at the output of peaking amplifiers are extracted through diplexer circuits that was designed to separate the fundamental signals and their second harmonics [8]. Those signals turn up at the output of peaking amplifier 1 are led to the input of the carrier amplifier. The peaking amplifier 2 generates IM2 and IM4 signals that are directed to the output of the carrier amplifier. The IM2 and IM4 signals are tuned in amplitude and phase by the amplifier and phase shifter over two paths as given in Fig. 1. The signals are inserted at the carrier amplifier by the diplexers.

Two-tone test of three-way Doherty amplifier at frequencies 2.139GHz and 2.141GHz gives result of linearization in Fig. 3. It compares output spectra before and after the linearization in case of 33dBm output power of each fundamental signal. It can be noticed that IM3 and IM5 products are suppressed for 15dB and 5dB, respectively.

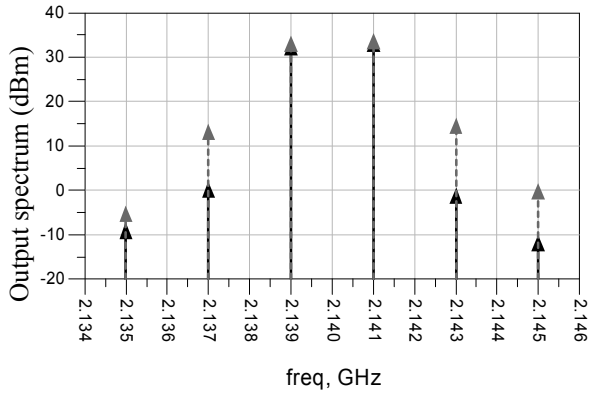

Fig. 3. Output spectra of three-way Doherty amplifier for device size ratio 1:2.5:2.5 for 33dBm average output power of fundamental signals; before (dashed line) and after the linearization (solid line) in case of 2MHz signal space

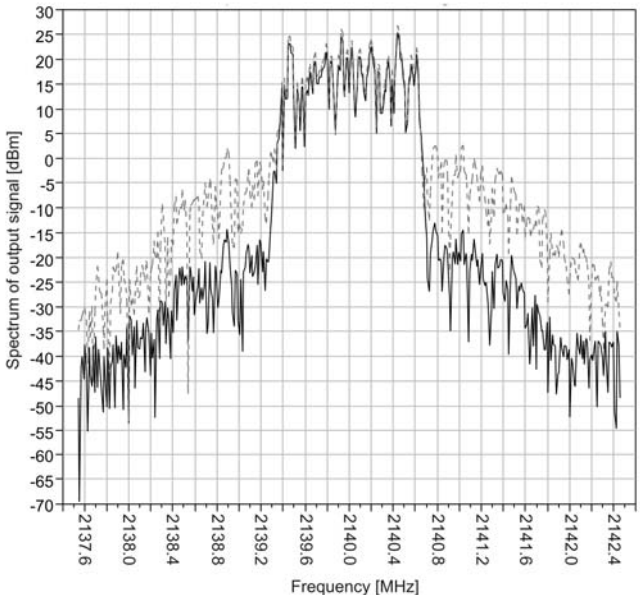

Fig. 4. Simulated spectrum of the output voltage for three-way Doherty amplifier for device size ratio 1:2.5:2.5 for OQPSK digitally modulated signal before (dashed line) and after linearization (solid line) for 35dBm output power

Fig. 2 shows that PAE in case of included consumption of the additional linearization circuit drops for 7.6% at 8dB back-off point (36dBm total output power) in reference to the case without linearization. However, PAE is outstanding in comparison with the case when the same devices (1:1:1 device size) were used for carrier and two peaking cells in Doherty amplifier with one quarter-wave transformer in output combining circuit [8]. For example, PAE of Doherty with linearization is 12.1% and 5.7% higher at 6dB and 12dB back-off, respectively, than in 1:1:1 device size configuration.

The output spectra obtained in simulation before and after linearization for OQPSK digitally modulated signal with 1.25MHz spectrum width, carrier at frequency 2.14GHz with output power 35dBm are compared in Fig. 4. It should be noticed that peak-to-average power ratio in this case is 6dB. For 35dBm average output power (9dB back-off), ACPR at two offsets (±900kHz and ±2100kHz) is improved for approximately 15dB. It follows from Fig. 2 that PAE at this power level is 27.7% that is 10.9%

higher that PAE obtained in [8] for 1:1:1 device size ration and different output combining circuit.

The results from Fig. 5 show the effects of three-way Doherty amplifier linearization at ±900kHz and ±2100kHz offsets from carrier frequency over 30kHz bandwidth accomplished within the output power range 27dBm to 37dBm. These results are compared to the case when linearization is not carried out. The presented results relate to the case when the amplitudes and phases of IM2 and IM4 signals are adjusted on the optimal values at 35dBm output power. It is evident from the figure that the linearization with the proposed approach gives satisfactory results in improvement of ACPR for ±900kHz offsets in the range of output power (approximately 29dBm-36dBm). It is noticed that ACPR improvement at ±2100kHz offsets is asymmetrical and exists in narrower power range, but generally observed ACPR is lower than for ±900kHz offsets in whole considered power range.

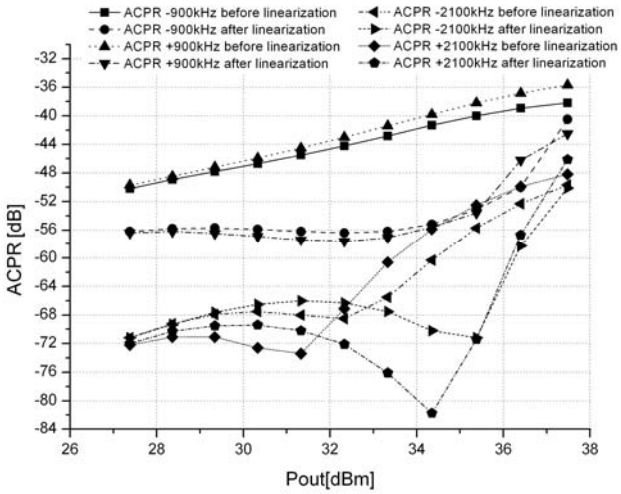

Fig. 5. ACPR before and after linearization of three-way Doherty amplifier for a power range at ±900kHz and ±2100kHz offsets from carrier frequency

III. CONCLUSION

This paper presents the linearization of three-way Doherty amplifier by the simultaneous injection of the second harmonics and fourth-order nonlinear signals (IM2 and IM4) at the input and output of the carrier amplifier. Those signals are generated at the output of peaking amplifiers that are biased at different points to produce adequate amplitude and phase relations between IM2 and IM4 signals. The three-way Doherty amplifier was designed with LDMOSFETs in carrier and peaking amplifies in periphery relations 1:2.5:2.5. The output impedances of the amplifier cells were selected to satisfy the output power relations between the carrier and peaking cells and to enable that the transmission lines in the output combining circuit are practical for realization.

For the three-way Doherty amplifier the linearization approach achieves very good results in the reduction of both IM3 and IM5 products retaining the high efficiency of Doherty amplifier (37.7% at 6dB back-off point).

On the top of that, since the peaking amplifiers were exploited as sources of signals for Doherty amplifier linearization there is no need for the additional nonlinear sources, which leads to lower energy consumption and simpler linearization circuit topology**.**

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