Baseband PLL frequency synthesizer for LDR UWB transmitter

Dušan Grujić, Jelena Popović, Milan Savić

***Abstract* — Baseband PLL frequency synthesizer is designed for low data rate UWB transmitter. Robust performance in case of expected process and operating conditions variation is ensured by design. Low power, area efficiency and compliance with standard digital CMOS process is considered and embedded into design constraints. Simulated PLL startup performance is presented.**

***Keywords* — PLL, frequency synthesizer, UWB, 90 nm CMOS.**

I. INTRODUCTION

The need for low power, low range and low cost communications in unlicensed part of spectrum is steadily growing. Wide variety of standards has been proposed and implemented such as Bluetooth, Zigbee and others. Ultra wideband (UWB) is an emerging technology intended to operate in 3 to 5 and 6 to 10 GHz bands and to fulfill all of these demands. Additional features, such as ranging should make UWB even more attractive for wide variety of applications. Low data rate UWB [1] transmitters are particulary interesting in area of wireless sensor data acquisition, such as radio system for telemedicine described in literature [2]. Although the UWB is a new technology, there are silicon verified proof of concept designs – literature [3].

Basic building block for UWB transmitter is the baseband PLL frequency synthesizer. The need for low cost demands single chip solution implemented in standard digital CMOS process. Nanometer scale processes, such as TSMC 90 nm used in this design, allow integration of both baseband and RF blocks. The topic of this paper is focused on baseband PLL design and simulation.

The paper is organized in three main sections. PLL requirements section considers the required performance and possible solutions to suit the applications and to be in accordance with standard. PLL design section deals with the design process details and individual block requirements and solutions. This section also considers the important aspects of robust design in case of large process and operating conditions variation. Finally, simulated PLL performance section presents the expected performance of design.

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II. PLL REQUIREMENTS

Baseband PLL frequency synthesizer requirements are made in accordance with IEEE 802.15.4a [1] draft. Output frequency is fixed and equal to cipher rate, which is 499.2 MHz for low data rate transmitter. Input frequency is chosen to be 31.2 MHz. Diverse UWB applications, for example wireless sensors or automotive, require a very wide operating temperature range of -40 to 125 °C. Cost-sensitive UWB applications demand an area-efficient solution in standard digital CMOS process. Low power nature of intended UWB applications impose a constraint on current consumption in order to maximize battery life. Current consumption requirement is set to 200 μA. Large channel spacing and spectral mask [1] relax the phase noise requirements and allow phase noise/power tradeoffs. Ring oscillator power, as one of the basic PLL building blocks, grows with number of stages n, while the phase noise exhibits $1/\sqrt{n}$ dependency [4], which makes it a good candidate for power/phase noise tradeoffs. Low power, relaxed phase noise and area efficiency constraints yield a five stage current-starved ring oscillator VCO.

Low duty cycle transmission modes and infrequent data transmission of intended applications gives the possibility for further power reduction. If the PLL can turn on and reach the steady state fast then it can be switched off in idle periods. Due to relatively low reference frequency, which is inherently tied to startup time in classic integer-N PLL, it is decided not to utilize low duty cycle transmission modes for power reduction. Speeding up the start-up process in order to switch off the PLL during low duty cycle transmission modes is a field for further research. Required PLL startup time is set to be at most 10 μs. Table 1 summarizes the PLL requirements.

TABLE 1: PLL REQUIREMENTS

Parameter	***Value***
Input frequency	31.2 MHz
Output frequency	499.2 MHz
Temperature range	-40 to 125 °C
Supply voltage	1.1 to 1.3 V
Current consumption	max 200 μA
Start-up time	max 10 μs

III. PLL DESIGN

Based on the data given in Table 1 PLL architecture and individual blocks are designed. Design procedure is given in the following text. Design steps are taken in exact order as listed.

A. PLL architecture

Chosen PLL architecture is shown in Fig. 1.

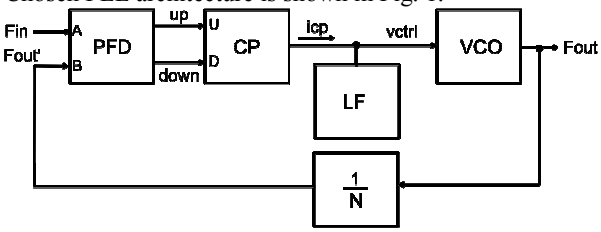

Fig. 1. PLL architecture

Figure 1 shows classic integer-N PLL structure. In order to keep the design simple and to keep the phase noise under control 2nd order loop filter (LF) was chosen, which gives a 3rd order PLL. Phase-frequency detector (PFD) is designed with dead zone avoiding logic [5]. Eliminating dead zone is important to suppress the sub-harmonic output frequency components. Charge pump is designed as controlled current source [5] with 18 µA current. Frequency divider is designed with four T flip-flops to get the required division ratio of 16. Voltage controlled oscillator and loop filter design require special attention to get reliable design across process and operating conditions variations.

B. VCO design

Voltage controlled oscillator architecture is set in PLL requirements section based on the design tradeoffs. Five stage current starved ring oscillator is well known configuration [6]. Major VCO design task is to ensure that it can generate required range of output frequencies and to keep the K_{VCO} in reasonable limits across process and operating conditions variations. Ensuring that the VCO operates correctly across process variations can be a difficult task, especially in nanometer scale technology where the expected variations are fairly large. With the architecture already set the only design parameters left are transistor widths W and lengths L. Minimum length transistors (100 nm in used technology) shouldn't be used in order to make the design robust to interconnection parasitic capacitance and to lower the flicker noise. Transistor dimensions also affect the required control voltage for nominal output frequency. Robust VCO should output the nominal frequency at control voltage which is half the supply voltage – in this case 600 mV. This constraint ensures that the control voltage has maximum headroom to compensate for process variations. Design that satisfies given constraints is produced after a few iterations. Output frequency is simulated by applying ramp signal with 1V/µs slope to control voltage input. Cadence Spectre simulation result is given in Fig 2.

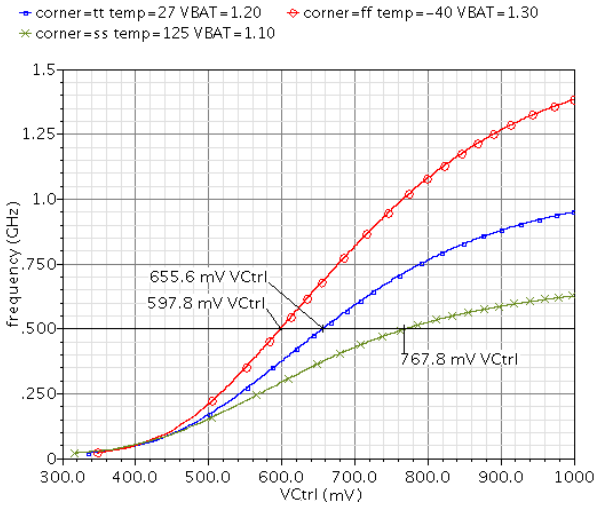

Fig 2. VCO output frequency simulation results

Figure 2 shows output frequency in slow (circles), typical (box) and fast corners (x mark). It can be seen that the VCO can generate the required frequency in all process and operating condition corners. Control voltage variation is also acceptable. Linear PLL model analysis require the VCO small signal gain K_{VCO}, which is shown in Fig. 3. Figure 3 shows that the K_{VCO} parameter varies from 900 MHz/V in slow case to 3.2 GHz/V in fast case. Such variation is expected and common in very wide operating conditions and process variations. Figures 2 and 3 show the performance of *optimized* VCO, and they present a clear picture of VCO sensitivity. This insight puts a great emphasis on careful design.

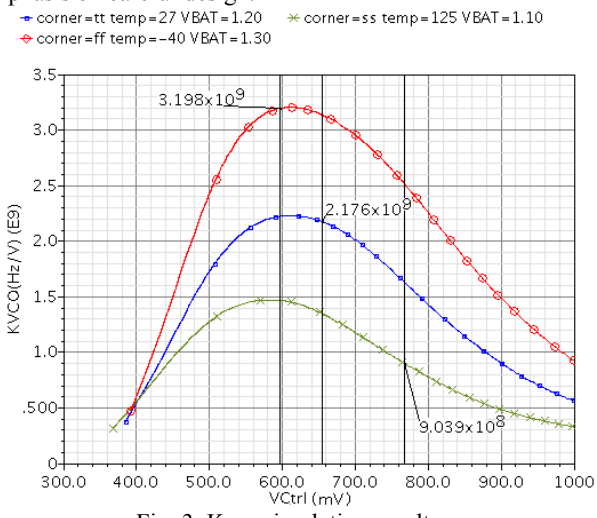

Fig. 3. K_{VCO} simulation results

C. Loop filter design

Third and higher order PLLs require carefully designed loop filters in order to preserve stability and desired transient behavior. Loop filter used in this design is given in fig. 4. Design procedure given in [7] is well suited for IC design because it allows the designer to choose an integer capacitor ratio.

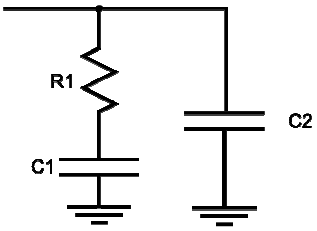

Fig. 4. Loop filter schematic

Loop filter is designed to have maximum phase margin of 60° at transition frequency [7]. This feature ensures that the phase margin will be sufficient across element tolerances, which are significant. Figure 5 shows the PLL open loop response with designed LF.

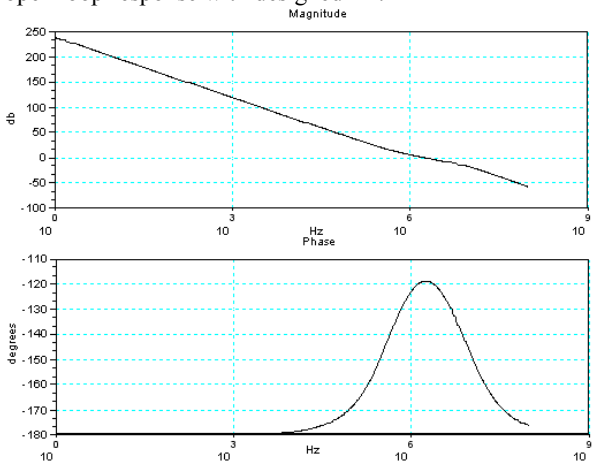

Fig 5. PLL open loop frequency response

Simulations were performed to determine the minimum phase margin in all possible combinations of tolerances. It is determined that the PM is always greater than 45°.

IV. SIMULATED PLL PERFORMANCE

Designed PLL performance is evaluated by transient startup simulation. The purpose of this simulation is to determine if the PLL has the desired transient response – startup time, quality of behavior (such as overshot) and current consumption. Indirectly the loop stability is also observed. Loop filter capacitor initial conditions were set to 0V in order to simulate the PLL turn on process. Simulation was performed with Cadence Spectre simulator with TSMC 90 nm RF technology. Figure 6 shows the PLL output frequency and table 2 shows the average current consumption in locked state.

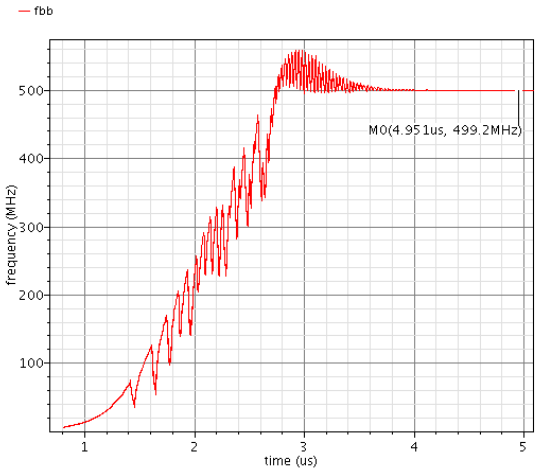

Fig. 6. PLL output frequency in startup process

TABLE 2: CURRENT CONSUMPTION

Block	***Average current [µA]***
PFD	8.2
CP	18.3
VCO	118
DIV16	27.5
Σ	**172**

V. CONCLUSION

This paper presents the baseband PLL frequency synthesizer for UWB. Design requirements and tradeoffs are tailored to accommodate the UWB standard and intended application needs. Transistor level simulation results show that typical startup time is less than 5 µs, and that the typical current consumption is well below the requested. Robustness to process and operating conditions variation is achieved by careful block design and architecture.

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